

ASYMMETRICAL DEVICES FOR SHORT GATE LENGTH PERFORMANCE WITH DISPOSABLE SIDEWALL

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] This invention relates to a field effect transistor (FET) with an implant within the gate length of the FET and a method of making the FET.

BRIEF DESCRIPTION OF THE PRIOR ART

[0002] It has been found that there are advantages for an FET to have an implant in the channel region that does not extend from the source to the drain and is aligned to the gate edge. For example, a pocket implant can be used to reduce short channel length effects. Yet, it can be undesirable to have a pocket implant extend into the source/drain (S/D) area because of resulting increased junction capacitance. It has also been found that there are advantages for an FET to have a region of controlling V_T on the source side of the channel with a more conductive V_T on the drain side. The short effective channel length and low source resistance of such an FET results in increased drive current and the reduced influence of the drain provides superior short channel characteristics. In the prior art, angled implants and lateral diffusions have been used to obtain channel impurity profiles self-aligned to the gate edge. However, these approaches have disadvantages resulting from restrictions in the channel implant profiles that can be obtained and from

the interdependence of the channel profile and the S/D extension profiles. It is therefore apparent that transistors having an independent channel implant region that is self aligned to the S/D edge is highly desirable.

SUMMARY OF THE INVENTION

[0003] In accordance with the present invention, there is provided a technique for fabrication of FET devices having a well controlled implant region between the two source/drain regions, self aligned to the S/D edge as well as the FET itself. In one embodiment, this implant region is used to create a controlling V_T region of shorter effective length than the S/D spacing. Preferably, the controlling V_T region is on the source side of the space between source and drain. In a second embodiment, the implant region is a pocket implant with limited extension into the S/D region. In a third embodiment, the implant is a S/D extension implant with extension into the channel region being independent of the diffusion of the S/D implant. The term “controlling V_T region” as used herein refers to that region which is the least conducting region and thus controls the current flow. For an n-channel transistor, this will generally be the more positive (higher) V_T . The controlling region could have a positive V_T and the rest of the channel could have a negative V_T , or the controlling region could have a negative V_T with the rest of the channel having a more negative V_T . The same applies for p-channel transistors except for a polarity reversal.

[0004] In accordance with the present invention, there is provided a fabrication technique for fabrication of FET devices having a well controlled sub-lithographic effective gate length, independent of gate orientation. The shorter effective channel length provides increased drive current since drive current is inversely proportional to channel length. The shorter effective channel length is achieved without requiring that the physical gate also be as short as the effective channel length. This provides superior short gate length

device characteristics and avoids the problems inherent in requiring the shorter gate length during fabrication of the device.

[0005] One way to achieve the effective short channel is to use a disposable gate process with masked/disposable sidewalls. This is accomplished by providing a doped substrate having spaced apart source/drain regions with a pad oxide and a patterned mask over the source/drain regions, preferably of silicon nitride, leaving the gate region exposed after disposal of the disposable gate. A removable sidewall is formed on the mask, preferably with silicon nitride, and the remaining gate region between the disposable sidewalls is filled with silicon dioxide with the surface then being planarized, preferably with a chemical mechanical polish (CMP). The sidewall adjacent to the source region is then removed by depositing and patterning a resist over the planarized surface and etching. A high V_T implant is then performed through the space from which the sidewall was removed to dope the channel region adjacent to the source region. The remaining sidewall is then removed. This is followed by a low V_T implant in the channel region between the source and drain regions. It should be understood that the high V_T implant can be a counter doping of the low V_T implant with appropriate masking to perform the implants in this manner. The result is an effective channel length, L , which is independent of the original disposable gate length. Fabrication then proceeds in standard manner to complete the device.

[0006] As a second embodiment, the low V_T channel implant can be performed initially after removal of the disposable gate and formation of disposable sidewalls on the mask as in the first embodiment, the sidewall on the source side is retained and the sidewall on the drain side is removed with appropriate deposition and patterning of resist and etching. A

low V_T is then provided into the exposed portion of the channel. The remaining sidewall at the source end of the channel is then removed and a high V_T implant is then provided of opposite conductivity type to the low V_T implant to provide the same result as in the first embodiment. Fabrication then proceeds in standard manner to complete the device.

[0007] As a third embodiment, it is desirable to add a liner over the mask surface, sidewalls and pad oxide prior to fabrication as noted above with reference to the first and second embodiments. The liner is preferably silicon nitride. The liner aids etch selectivity and protects the surface of the silicon when performing the implants.

[0008] As a fourth embodiment, the FET can be made symmetrical rather than asymmetrical as described in the first and second embodiments with a different implant in the center of the channel region relative to the source and drain ends of the channel region. An implant can be performed following sidewall formation. The sidewalls would then be removed and the entire channel region would be doped n- or p-type to provide either a less heavily net doped region adjacent the source and drain regions if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain if the opposite conductivity type dopant is used. The resist pattern used to mask removal of selected sidewalls can also distinguish n- and p-channel transistors for different V_T implants. Optionally, an implant can be performed before formation of the sidewalls, followed by an implant after formation of the sidewalls. For this option, the sidewall can be left in place for formation of the actual gate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGURES 1A to 1D represent a process flow for formation of an asymmetrical FET device for short gate length performance in accordance with a first embodiment of the present invention;

[0010] FIGURES 2A to 2C represent a process flow for formation of an asymmetrical FET device for short gate length performance in accordance with a second embodiment of the present invention;

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[0011] FIGURE 3 shows a step in the process flow in accordance with a third embodiment of the present invention;

[0012] FIGURES 4A and 4B show a process flow for formation of a symmetrical FET device for short gate length performance in accordance with a fourth embodiment of the present invention;

[0013] FIGURES 5A to 5C show a process flow for formation of an FET in accordance with a fifth embodiment of the present invention; and

[0014] FIGURES 6A and 6B show a process flow for formation of an FET in accordance with a sixth embodiment of the present invention.

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DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] In accordance with a first embodiment of the invention, the effective short channel is achieved by using a disposable gate process with masked/disposable sidewalls as shown in FIGURES 1A to 1D. For an n-channel device (it is understood that all conductivity types will be opposite for a p-channel device), there is provided a p-doped substrate 1 having spaced apart source/drain regions 3, 5 with a pad oxide 7 over the substrate and a patterned silicon nitride mask 9 over the source/drain regions. This arrangement is provided, leaving the gate region exposed after prior disposal of the disposable gate in standard manner as shown in FIGURE 1A. A removable polysilicon sidewall 11, 13 is formed on each side of the nitride mask 9 and the remaining gate region between the disposable sidewalls is filled with silicon dioxide 15 with the surface then being planarized, preferably with a chemical mechanical polish (CMP) as shown in FIGURE 1B. The sidewall 11 adjacent what will ultimately be the source region is then removed by depositing and patterning a resist over the planarized surface and etching in standard manner. A high V_T implant is then performed through the space from which the sidewall was removed to dope the channel region 17 adjacent to the source region 3 as shown in FIGURE 1C and the silicon dioxide 15 and remaining sidewall 13 are then removed. This is followed by a low V_T implant in the channel region between the source and drain regions to leave the high V_T region 17 adjacent to the source region 3 and a low V_T region 19 adjacent to the drain region 5 as shown in FIGURE 1D. Optionally, the low V_T implant can be performed before formation of the sidewalls.

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[0016] It should be understood that the V_T of region 17 is a result of the combination of what has been referred to as the high V_T and the low V_T implant. One can be a counter-

doping of the other. The result is an effective channel length, L , which is independent of the original disposable gate length. Fabrication then proceeds in standard manner to complete the device.

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[0017] As a second embodiment, the low V_T channel implant can be performed prior to the high V_T implant. After removal of the disposable gate, disposable sidewalls are formed on the mask as in FIGURE 1B of the first embodiment and as shown in FIGURE 2A wherein like reference characters refer to the same or similar structure. The sidewall on the source region side 11 is retained and the sidewall on the drain region side 13 is removed with appropriate deposition and patterning of resist and etching in standard manner. A low V_T implant is then provided into the exposed portion 21 of the channel as shown in FIGURE 2B. The remaining sidewall 11 at the source end of the channel is then removed and a high V_T implant is implanted into the channel region between the source and drain regions. Preferably, the high V_T implant is of opposite conductivity type to the low V_T implant to provide a high V_T region 23 and a low V_T region 21. Fabrication then proceeds in standard manner to complete the device. Optionally, the high V_T implant can be performed prior to formation of the sidewalls.

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[0018] As a third embodiment, it is desirable to add a liner 25 over the mask surface, sidewalls and pad oxide prior to fabrication as noted above with reference to the first and/or second embodiments and particularly over the structure as shown in FIGURE 1A and the structure as shown in FIGURE 2A prior to formation of the sidewalls 11, 13 with subsequent formation of the sidewalls 11, 13 over the liner as shown in FIGURE 3. The liner 25 is preferably silicon nitride. Fabrication then proceeds as in the prior embodiments as discussed above.

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[0019] As a fourth embodiment as shown in FIGURES 4A and 4B, the FET can be made in a symmetrical rather than asymmetrical embodiment as described in the first and second embodiments with a different implant 27 in the center of the channel region as shown in FIGURE 4A. Optionally, implant 27 may include a punch-through implant. The sidewalls 11, 13 are then removed and the entire channel region is doped with n- or p-type to provide either a less heavily net doped region adjacent the source and drain regions 29 if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain regions if the opposite conductivity type dopant is used and the opposite characteristic in region 27 as shown in FIGURE 4B. Optionally, the implant in the full channel region can be performed prior to sidewall formation. Fabrication then proceeds in standard manner to complete the device.

[0020] As a fifth embodiment as shown in FIGURES 5A to 5C, the FET can be made symmetrical with the implant in the channel regions adjacent to the source and drain being performed prior to the implant in the central region. As in the first embodiment, sidewalls 11 and 13 are formed and the central region 15 is filled and planarized as shown in FIGURE 5A. Sidewalls 11 and 13 are then removed and an implant is performed into regions 50. As depicted in FIGURE 5B, the implant regions 50 may be pocket implants. Optionally, source/drain extension or V_T adjust implants can be performed at this time. Center masking material 15 is then removed and an implant is performed into the channel region 52 between the source and drain regions.

[0021] As a sixth embodiment, the sidewalls are left in place, reducing the physical gate length, as shown in FIGURES 6A and 6B. An implant is performed in the full channel region 60 prior to formation of the sidewalls. A second implant is performed into region

64 after formation of the sidewalls, resulting in a different implant profile in regions 62 versus region 64. Sidewalls 11 and 13 can then be left in place as formation of the gate proceeds in normal fashion. Optionally, sidewall 11 or sidewall 13 can be removed with appropriate pattern and etch steps prior to or subsequent to the implant to region 64.

[0022] Optionally, the sidewall material can be of the same material as the masking material and left in place or removed with a timed isotropic etch prior to gate formation.

[0023] Though the invention has been described with reference to specific preferred embodiments thereof, many variations and modifications will immediately become apparent to those skilled in the art. For example, the opening for the damascene gate can be made by a trench etch into the masking material rather than by removal of a disposable gate. Various materials or stacks of materials can be used for the masking material, the sidewalls, and the fill material. The source/drain implants can be performed after the actual gate formation rather than with the disposable gate, and the edge of the source/drain implant relative to the opening for the damascene gate can vary from that shown, and a source/drain extension may be used. The implants into the various regions encompassed by the gate opening can include but are not restricted to threshold adjustment implants, source/drain extension implants, pocket implants and punch through implants. Multiple implants of different species or energy can be performed in any of the regions to obtain the desired doping profile. The depth of implants illustrated is not intended to be restrictive. Different sequences of sidewall formation, sidewall removal, and implantation, including multiple sidewall formation can be used. Sidewalls can be added after completion of the channel region implants to adjust the physical gate length.

It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modification.